LISTING OF THE CLAIMS

This listing of claims replaces all prior versions and listing of claims in the present application:

Claims 1-37 (canceled)

Claim 38 (Previously presented): A semiconductor device comprising a semiconductor substrate having therein a low-capacitance substrate region, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein:

a plurality of substrate openings are formed in said low-capacitance substrate region, penetrating at least an undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate.

Claim 39 (Previously presented): The semiconductor device according to claim 38 wherein a low-permittivity insulating material is embedded in said substrate openings.

Claim 40 (Previously presented): The semiconductor device according to claim 38, wherein a length of said substrate openings within said semiconductor substrate is equal to or larger than half a thickness of said semiconductor substrate, or said substrate opening penetrate said semiconductor substrate.

Claim 41 (Previously presented): The semiconductor device according to claim 38 wherein said substrate openings are randomly arranged as viewed normal to a surface of said substrate.

Claim 42 (Previously presented): The semiconductor device according to claim 38, wherein said substrate openings are formed so that no linear current path is formed crossing said low-permittivity substrate region as viewed normal to a surface of said substrate.

Claim 43 (Previously presented): The semiconductor device according to claim 38, wherein a high-permeability region is provided to overlie said low-permittivity substrate region, said high-permeability region including a high-permeability material embedded in an interlevel dielectric film.

Claim 44 (Previously presented): The semiconductor device according to claim 43, wherein said high-permeability region includes therein a plurality of high-permeability magnetic rods arranged and including said high-permeability material having an electric conductivity and embedded in respective film openings having an aspect ratio (ratio of depth to diameter or length of a side) of 1 or above, said film openings penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

Claim 45 (Previously presented): The semiconductor device according to claim 43, wherein said high-permeability region includes therein a plurality of high-permeability magnetic rods arranged and including said high-permeability material having an insulating property and embedded in respective film openings, said film openings penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

Claim 46 (Previously presented): A semiconductor device comprising a semiconductor substrate, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein a high-permeability region is provided in an interlevel dielectric film, wherein:

said high-permeability region includes therein a plurality of high-permeability magnetic rods including a high-permeability material embedded in respective film openings, said film openings having an aspect ratio (depth/diameter or a side) of 1 or above and penetrating at least one of said interlevel dielectric films to reach another of said interlevel dielectric films.

Claim 47 (Previously presented): The semiconductor device according to claim 46, wherein said high-permeability material has either an electric conductivity or an insulating property.

Claim 48 (Previously presented): The semiconductor device according to claim 46, wherein said high-permeability material is a composite material including a low-permittivity insulating material and a high-permeability magnetic material including an electric conductivity or an insulating property.

Claim 49 (Previously presented): The semiconductor device according to claim 48, wherein said low-permittivity insulating material is a porous insulating material.

Claim 50 (Previously presented): The semiconductor device according to claim 46, wherein said high-permeability magnetic rods include a high-permeability material film coating an inner wall surface of said insulating film openings and a low-permittivity insulating material embedded inside said high-permeability material film.

Claim 51 (Previously presented): The semiconductor device according to claim 46, wherein said high-permeability region includes a high-permeability magnetic plane overlying and/or underlying said high-permeability magnetic rods, said high-permeability magnetic plane having a material including a high-permeability material embedded in depressions formed in a surface of said interlevel dielectric film.

Claim 52 (Previously presented): The semiconductor device according to any one of claim 38, wherein an inductor is formed to overlie said low-permittivity substrate.

Claim 53 (Previously presented): The semiconductor device according to claim 46, wherein an inductor is formed to overlie said low-permittivity substrate region.

Claim 54 (Previously presented): The semiconductor device according to claim 52, wherein an analog circuit is formed on said semiconductor substrate in said low-capacitance substrate region.

Claim 55 (Previously presented): The semiconductor device according to claim 53, wherein an analog circuit is formed on said semiconductor substrate in an area including said high-permeability region.

Claim 56 (Previously presented): The semiconductor device according to claim 54, wherein a logic circuit is formed on said semiconductor substrate in an area other than an area in which said low-capacitance substrate region is formed.

Claim 57 (Previously presented): The semiconductor device according to claim 54, wherein a logic circuit is formed on said semiconductor substrate in an area other than an area in which said high-permeability region is formed.

Claim 58 (Previously presented): The semiconductor device according to claim 38, wherein an

on-chip antenna interconnect is formed on said low-capacitance substrate region.

Claim 59 (Previously presented): The semiconductor device according to claim 58, wherein said on-chip antenna interconnect is formed in a peripheral area of a semiconductor chip.

Claim 60 (Previously presented): The semiconductor device according to claim 58, wherein said on-chip antenna interconnect is formed in an I-character, L-character or U-character shape or in multiple loops.

Claim 61 (Previously presented): The semiconductor device according to claim 58, wherein said on-chip antenna interconnect is configured by interconnect layers embedded in slit-like openings which are formed to penetrate a plurality of said interlevel dielectric films.

Claim 62 (Previously presented): The semiconductor device according to claim 59, wherein a grounded shield interconnect is formed inside said on-chip antenna interconnect.

Claim 63 (Previously presented): The semiconductor device according to claim 62, wherein said shield interconnect is configured by interconnect layers embedded in slit-like openings formed to penetrate a plurality of said interlevel dielectric films.

Claim 64 (Previously presented): The semiconductor device according to claim 38, wherein an interconnect configured by a plurality of interconnect layers is provided in said low-capacitance substrate region.

Claim 65 (Previously presented): The semiconductor device according to claim 64, wherein said interconnect layers configure an inductor.

Claim 66 (Previously presented): The semiconductor device according to claim 64, wherein interconnects in said plurality of interconnect layers are connected electrically in parallel through a plurality of via-plugs.

Claim 67 (Previously presented): The semiconductor device according to claim 64, wherein ends of interconnects in said plurality of interconnect layers are connected together through a plurality of via-plugs so that said plurality of interconnect layers are connected electrically in series.

Claim 68 (Previously presented): The semiconductor device according to claim 67, wherein a current flowing through first interconnects formed in one of said interlevel dielectric films and a current flowing through second interconnects formed in another of said interlevel dielectric films adjacent to said one of said interlevel dielectric films do not flow opposite to each other.

Claim 69 (Previously presented): The semiconductor device according to claim 67, wherein a first interconnect layer formed in one of said interlevel dielectric films and a second interconnect layer formed in another of said interlevel dielectric films adjacent to said one of said interlevel dielectric films conduct currents in the same direction in the structure wherein said plurality of interconnect layers are connected in series.

Claim 70 (Previously presented): The semiconductor device according to claim 67, wherein interconnects of a first interconnect layer formed in one of said interlevel dielectric films and interconnects of a second interconnect layer formed in another of said interlevel dielectric films adjacent to said one of said interlevel dielectric films do not extend overlapping each other as viewed in the vertical direction in the structure wherein said plurality of interconnect layers are connected in series.

Claim 71 (Previously presented): The semiconductor device according to claim 38, wherein contact plugs configuring electrodes of said transistor and an insulating film containing at least silicon are formed on one of said interlevel dielectric films in said low-permittivity substrate region, said insulting film having constituent atoms and composition different from those of said one of said interlevel dielectric films.

Claim 72 (Previously presented): The semiconductor device according to claim 38, wherein an insulating containing at least silicon is formed in said low-permittivity substrate region on one of said interlevel dielectric films receiving therein contact plugs configuring electrodes of said transistor, said insulating film having constituent atoms and composition difference from those of said one of said interlevel dielectric films.

Claim 73 (Previously presented): The semiconductor device according to claim 38, wherein said low-permittivity insulator rods have a topmost surface located lower than a topmost surface of contact plugs in said low-capacitance substrate region.

Claim 74 (Previously presented): The semiconductor device according to claim 38, wherein an insulating film is disposed to cover said low-permittivity insulator rods, said insulating film having a higher permittivity and higher mechanical strength than another insulating film embedded in said rods.

Claim 75 (Withdrawn): A method for manufacturing a semiconductor device including a semiconductor substrate, a transistor formed on a surface area of said semiconductor substrate, and a multi-layered interconnection structure including a plurality of interlevel dielectric films and a plurality of interconnect layers overlying said transistor, wherein a high-permeability region is provided in said interlevel dielectric film, said method comprising the consecutive steps of:

(1) forming the transistor on said semiconductor substrate;

(2) forming a plurality of substrate openings penetrating at least undermost one of said interlevel dielectric films to reach an internal of said semiconductor substrate;

(3) embedding an insulating material in said openings; and

(4) grinding a bottom surface of said semiconductor substrate.

Claim 76 (Withdrawn): The method according to claim 75 wherein said insulating material embedded in said step (3) is low-permittivity insulating material having a lower permittivity than silicon oxide.

Claim 77 (Withdrawn): The method according to claim 75, further comprising, between said step (1) and said step (2), the additional step of forming an interlevel dielectric film covering said transistor on said semiconductor substrate.